ESSDERC 2010 - Seville, Sept.13th, 2010

Nanoelectronics: a tool to face the future

Date of the Tutorial: September 13th, 2010, Seville - during ESSDERC-ESSCIRC'2010
Organized by: Francisco Gámiz and Andrés Godoy, University of Granada

Abstract:
The aim of this Tutorial is to present the status and trends of different hot topics in the field of nanoelectronics. All the presentations will consist on a 50 minutes oral presentation + 10 minutes of questions.

Programme

9:20 – 9:30 Introduction
F. Gámiz and A. Godoy, University of Granada

9:30 – 10:30
• CMOS process variability – from technology to circuits and systems
J. Lorenz, Fraunhofer Institute, Germany

10:30 – 11:00 BREAK

11:00 – 12:00
• Industrial challenges for the CMOS technology to reach the 22nm and 16nm nodes
T. Skotnicki, STMicroelectronics, France

12:00 – 13:00
• 1T-DRAM structures
Sorin Cristoloveanu, IMEP-LAHC, France

13:00 – 14:30 LUNCH

14:30 – 15:30
• III-V devices for high frequency applications
Tomás Palacios, MIT

15:30 – 15:45 BREAK

15:45 – 16:45
• Silicon nanowires
T. Ernst, CEA-LETI, Grenoble, France

16:45 – 17:45
• Carbon based Nanoelectronics: Carbon Nanotubes & Graphene as drivers to device innovation and Post-CMOS area.
Sthephan Roche, CEA, INAC, SP2M, Grenoble, France

Title: CMOS Process Variability – from Technology to Circuits and Systems

Abstract

Process variations belong to the most critical challenges for the further scaling of nanoelectronic devices, as highlighted among others in various sections of the International Technology Roadmap for Semiconductors ITRS. In order to meet this challenge, sources of variability must be identified, their size must be quantified, and their impact on devices, circuits and systems assessed and compared to the specifications of the products in terms of variations or performance.

The impact of process variations on device and circuit performance cannot be studied mainly with experiments: This would require the capability to sufficiently control the process variations, in order to study the impact of one varying process parameter while all other parameters are kept at their nominal value. Besides the required unacceptably large experimental effort, this approach is mostly not possible at all, because variations like Line Edge Roughness can due to physical reasons not be fully suppressed. Moreover the variations can hardly be measured in-situ and non-destructively during the fabrication of a device, which means that it is not possible to identify for a specific device in question how large the process variations actually were which occurred during the fabrication of this specific device.

In contrast to the experimental approach, the missing direct link between process variations occurring during the fabrication of a device and the performance of the final device, circuit or system could very well be established and quantified by the use of process, device, circuit and behavioral simulation: If the simulation tools used employ sufficiently accurate physical models and are well calibrated to match and reproduce the “nominal” process, one can easily introduce intentional variations of one or more process parameters, simulate the impact of the variations on the fabrication process in question, and then trace the impact of that modified process through all following process steps to the final devices. Device, circuit and behavioral simulation can then be applied to extract the parameters determining the device, circuit and system performance, like threshold voltage, on- and off-current, frequency, and to quantify the variations of such parameters caused by the process variations being studied.

Existing software platforms fall short of meeting the challenge of simulating variations from their sources at process level to their impacts on devices, circuits and systems: Whereas many very good results were published in some specific areas like dopant fluctuations, other key effects for industrial applications were hardly studied, and a full simulation sequence is still missing. The obvious complexity problem can only by resolved by a hierarchical approach.

In this presentation, first the main sources of variability in CMOS processes are summarized, including especially effects from patterning and annealing steps with are neglected in most other presentations. The state-of-the-art and main limitations of simulation tools available are discussed. Here, a key problem is the insufficient interfacing and integration between tools dealing with the different simulation areas lithography/topography, doping, device, circuit, and system. Finally, examples for the results of hierarchical simulation of process variability at device, circuit and system level are presented. Especially it is demonstrated that different device architectures may lead to completely different responses to the same process variation, including highly asymmetric variations resulting at device level from a symmetric variation at process level.

Jürgen Lorenz; Fraunhofer Institut, Erlangen, Germany

Biography

Dipl.-Phys. Dipl.-Math. Jürgen Lorenz joined Fraunhofer in 1983. Since 1985 he is in charge of the technology simulation department of the then newly founded IISB. His main subjects are the development of physical models and programs for semiconductor process simulation and the required algorithms, in which field he also completed his Ph.D. (Dr.-Ing.). He authored or co-authored more than 100 papers, and has repeatedly been or is member of the technical committees of the ESSDERC, SISPAD, and IEDM conferences. During the last 20 years he has been involved in more than 25 European projects, of which he acted as coordinator for ESPRIT PROMPT and PROMPT II, IST MAGIC_FEAT, the network NEWSSTAND, and the ESPRIT User Groups UPPER and UPPER+, and the SSA SUGERT. Following requests from industry he contributes since 2000 as expert to the preparation of the International Technology Roadmap on Semiconductors, and is chairman for its Modeling and Simulation Chapter since 2002.

Title: Industrial challenges for the CMOS technology to reach the 22nm and 16nm nodes

Abstract

The continuous scaling of CMOS technologies has enabled them to address still more and new applications. Communication, computer, consumer, automotive, industrial, security, medical and many other products benefit from a continuously increasing functionality and data and signal processing capability per chip. This trend has also driven an increasing need to reduce and manage power consumption of related chips. After a brief period of stagnation in frequency increase due to excessive power dissipation, today the course towards higher clock frequency is back again. The so called Low Power technologies are required to offer higher and higher speed. Both parallel computing and frequency increase are put on the table of designers. In this Tutorial, we will thus review the most advanced technological solutions to provide industrially viable and competitive CMOS process for the next 22nm and 16nm nodes. At the first step, historical review of past and existing CMOS nodes will be carried out, focusing on limitations and employed solutions. We will next focus on the oncoming 22nm and 16nm nodes, from the standpoint of the power, performance and dimension scaling. Growing concerns with variability and electrostatics will be evaluated. We will also benchmark different device structures such as Bulk, FDSOI and FinFET and prospect on their suitability for maximizing performance at minimum power. Other advanced process modules will also be evaluated such as mechanical strain, as well as some circuit-device level solutions such as Body Biasing, and other performance and power management techniques. Striving for high performance at low power has become today an economic, environmental, and political consideration. Electronic tools and devices are known to consume an important and increasing amount of the entire energy produced by the industrial world. Hence, to make electronics “greener” without compromising its efficiency is becoming the next huge challenge for the entire IC industry.

Thomas Skotnicki; STMicroelectronics, France

Biography

Thomas SKOTNICKI is the STMicroelectronics Fellow and Director of Advanced Devices at STMicroelectronics Crolles, France, that he joint in 1999. Before, from 1985 till 1999, he was with France Telecom R&D (*CNET-Centre National d’Etudes des Telecommunications*). He received his Master and EE degrees from the Warsaw University of Technology in 1979, the PhD diploma from the Institute of Electron Technology, Warsaw Poland in 1985, and in 1993 he received the HDR (Habilitated for Directing Research) diploma from the *Institut National Polytechnique de Grenoble,* France. In 2007, he received the title of Professor from the President of Poland. The current focus of his program at STMicroelectronics is on Low Power / Low Variability for 22nm and beyond CMOS, on innovative device structures, new memory concepts and cells, and on integration of new materials for CMOS. Among his own and his team, main scientific and R&D achievements (inventor or co-inventor) are: the VDT (Voltage-Doping Transformation) technique and MASTAR models (MASTAR served for calculating the ITRS 2003, 2005, 2007 and 2009 CMOS Roadmaps), silicon devices showing large dynamic NR (negative resistance) in room temperature, the SON (Silicon-On-Nothing) technology (awarded Rappaport Award for the best IEEE EDS publication of year 2000), capacitor-less Bulk DRAM cell, Totally Silicided (TOSI) metallic gate technology, Double Gate (DG) gate SON technology, "dielectric pockets" technology (awarded ESSDERC 2000 Best Paper), etc. He holds about 60 patents on new devices, circuits and technologies. He has presented over 50 Invited Papers and Short Course Lectures, co-edited one book, (co-) authored about 300 scientific papers (review based), and several book chapters in the field of CMOS devices and circuits. From 2001 to 2007, he served as Editor for IEEE Transactions On Electron Devices. He has been teaching at EPFL (Lausanne) and INPG (Grenoble), and has supervised and led to successful defence more than 20 PhD theses. He has been serving in numerous Conference Program and Executive Committees (IEDM, VLSI, ESSDERC, ECS, SNW, IWJT), Academia Advisory Boards, Governmental Expert Commissions, R&D Program Steering Committees, and ITRS. He is an IEEE Fellow and SEE Senior Member.

Title: Capacitorless 1T-DRAM SOI Structures

Abstract

The DRAM evolution is facing severe challenges due to the difficulty to further scale down the storage capacitor. A revolutionary solution is to suppress the capacitor and use the floating body of a transistor to store the charge. The architecture and operation mechanisms of SOI transistors make realistic the advent of such capacitor-less single-transistor memory cell (1T-DRAM). Several types of 1T-DRAMs have already been proposed and will be critically compared. They all take advantage of the floating-body, electron-hole coupling, injection, and retention mechanisms in SOI. The basic idea is that the minority carrier current is sensitive to the amount of majority carriers stored in the transistor body.

Two innovative concepts, MSDRAM and A-RAM, will be described in detail. The MSDRAM features double-gate operation and achieves strong hysteresis, long retention, large memory window and low power. The A-RAM is a multiple body device, compatible with ultimate scaling and single-gate operation: one body serves to generate and store the charge, while the second body acts as a charge detector. The performances and advantages of A-RAM and MSDRAM will be outlined. The discussion is based on preliminary measurements and systematic simulations. Pragmatic solutions for programming and retention optimization will be discussed in terms of device technology and architecture. We will show that these devices are versatile, adaptable to planar or vertical configurations. They can also be envisioned for enriched functionalities: 'unified' memory with volatile and non-volatile capability, and multi-bit memory.

Sorin Cristoloveanu; IMEP-Minatec Grenoble, France

Biography

Sorin Cristoloveanu received the PhD (1976) in Electronics and the French Doctorat ès-Sciences in Physics (1981) from Grenoble Polytechnic Institute, France. He is currently Director of Research CNRS. He also worked at JPL (Pasadena), Motorola (Phoenix), and the Universities of Maryland, Florida, Vanderbilt, and Western Australia. He served as the director of the LPCS Laboratory and the Center for Advanced Projects in Microelectronics, initial seed of Minatec center. He authored more than 700 technical journal papers and communications at international conferences (including 130 invited contributions). He is the author or the editor of 22 books, and he has organized 18 international conferences. His expertise is in the area of the electrical characterization and modeling of semiconductor materials and devices, with special interest for silicon-on-insulator structures. He has supervised more than 60 PhD completions. With his students, he has received 8 Best Paper Awards, an Academy of Science Award (1995), and the Electronics Division Award of the Electrochemical Society (2002). He is IEEE Fellow, Electrochemical Society Fellow, ‘World Class University’ Professor, and Editor of Solid-State Electronics.

Title: III-V devices for high frequency applications

Abstract

The combination of the unique properties of III-V semiconductors with the new tools offered by nanotechnology enables unprecedented opportunities for the development of high frequency electronic devices. The recent announcements of transistors with operating frequencies above 1 THz, sub-mm wave GaN devices with breakdown voltages of more than 100 V, and MMIC circuits operating above 600 GHz are quickly changing the limits and possibilities of high frequency electronics. This lecture will review the current state-of-the-art of high speed transistors based on III-V semiconductors. The main design trade-offs and technologies required for these devices will be studied, as well as how parasitic resistances and capacitances can ultimately limit their performance. The lecture will finish with a review of new technologies and structures, such as nanowires and multi-gate devices, with the potential to push the performance of these transistors even further. All these developments will be put in the framework of several target applications, including RF electronics, beyond-Si digital circuits and new devices for energy harvesting.

Tomás Palacios, MIT, Massachussets, USA

Biography

Prof. Tomás Palacios leads the Advanced Semiconductor Materials and Devices Group at the Massachusetts Institute of Technology. His research focuses on the development of new electronic devices to advance the fields of information technology, biosensors and energy conversion. His work has been recognized with multiple awards including, the 2010 Young Scientist Award of the International Symposium on Compound Semiconductors, the 2009 ONR Young Investigator Award and the NSF CAREER Award, the 2008 DARPA Young Faculty Award, the Young Researcher Award at the 6th International Conference on Nitride Semiconductors, and the Best Student Paper Award at the 63rd IEEE Device Research Conference. Prof. Palacios received his PhD from the University of California – Santa Barbara in 2006, and he has authored more than 130 contributions on advanced semiconductor devices, as well as numerous book chapters and patents.

Title: Silicon nanowires

Abstract

Multigates and thin film devices are needed to scale down CMOS transistors below the 22nn node. For those nodes, electrostatic integrity and variability should be reduced without any severe degradation of the driving current. Nanowire (NW) is seen as a natural scaling of multiple gate and thin film devices, leading to very promising performances.

In this short-course we will review different aspects of nanowire fabrication with top-down technologies. Various approaches for diameter control, channel shape and doping, gate stack process, S/D optimizations and pitch limitations will be presented. Then NW electrical behavior will be discussed based on experimental characterization including ION/IOFF compromise, as well as mobility, interfaces quality and surface orientation impact. At the end, an opening on new devices based on silicon nanowire intrinsic properties will be given. How Si nanowire can be beneficial to memories or sensors?

[1] T.Ernst et al. IEDM 2006, 2008 / [2] A. Hubert et al, IEDM 2009 / [3] K. Tachi et al, IEDM 2009

Thomas Ernst; CEA-LETI, Grenoble, France

Biography

Thomas Ernst received his Ph.D. degrees from the National Polytechnics Institute of Grenoble, France, in 2000. From 1997 to 2000, he developed advanced SOI CMOS electrical characterization, simulation and modeling methods at STMicroelectronics and IMEP laboratory. He then joined CEA-LETI to develop novel strained-channel CMOS architectures for 32 nm technology. In particular, he was leading strained SOI, strained Germanium, and SiGeOI CMOS integration at LETI. Since 2005, he is leading the 3D multi-channels and nanowire CMOS devices developments. His expertise is in the area of novel CMOS device fabrication technology and MOSFETs analytical modeling for electrical characterization. Dr. Ernst is author or co-author of over 130 technical journal papers and communications at international conferences on CMOS device integration, modeling and characterization. He is author or co-author of more than 15 patents. He is a member of ESSDERC and ULIS conferences technical committees since 2005 and member of IEDM TPC for 2 years. He is a recipient of research grant from the European Research Council to develop multi-physics integrated systems.

Title: Carbon-based Nanoelectronics: Carbon Nanotubes & Graphene as drivers to Device Innovation and POST-CMOS area.

Abstract

In this presentation, we will first briefly review the main physical properties of clean carbon nanotubes and graphene that constitute a new material family with strong potential for future nanoelectronics. Graphene is a two-dimensional monolayer of sp^2 bonded carbon atoms in a dense honeycomb crystal structure which behaves electronically as a zero-gap semiconductor with exceptional charge mobilities. Carbon nanotubes can be seen as folded graphene ribbons, and as one-dimensional nanoscale objects, they stand as outstanding ballistic conductors able to withstand considerably huge current densities, opening genuine perspectives for efficient interconnects.

The properties of carbon-nanotubes-based field effect transistors will be discussed in details with an emphasis on the nature of Schottky barriers which can be tuned either by the nanotube geometry, the surrounding electrostatic or the application of external magnetic fields. The sensing capability of carbon nanotubes devices will be also explained and illustrated.

In a second part, the engineering of innovative graphene-based devices will be shown to demand for a systematic use of chemical functionalization of the raw material (exfoliated or epitaxial graphene layers). New possible device principles based on quantum coherence and intrinsic randomness conveyed by chemical disorder (mobility gaps) will be discussed. Finally challenging research directions for the development of carbon-based spintronics, nanoelectromechanics or thermoelectrics will be outlined.

References

[1] J.C. Charlier, X. Blase and S. Roche, Rev. Mod. Phys. 79, 677 (2007).

[2] A. Cresti et al., Nano Research 1, 361-394 (2008).

Stephan Roche , CEA, INAC, SP2M, Grenoble (FRANCE)

Biography

Dr. Stephan Roche is a permanent research member of the Commissariat à l'Energie Atomique-CEA (Grenoble, FRANCE) working at the Institut of NAnosciences and Cryogenics (INAC, SP2M, L_sim). His research focuses on theoretical and computational nanosciences, more precisely quantum transport and computational modelling of low dimensional systems and complex materials. His expertise combines a broad variety of theoretical tools, allowing for the quantitative exploration of charge transport from the atomic to the mesoscopic scale. His scientific carrier took off at the CNRS in Grenoble (France); it continued at the Department of Applied Physics of Tokyo University in Japan and at the Department of Theoretical Physics at the University of Valladolid, Spain. In 2000, he was appointed as an Assistant Professor at University Joseph-Fourier, and further joined the CEA as a permanent researcher in 2004.

His research activities have yielded cutting-edge achievements in the fields of carbon nanotubes, DNA, graphene-based materials, and semiconducting nanowires. Dr. Roche has leaded and coordinated the development of various real space order N approaches to tackle with the computation of transport properties in complex systems. These methodologies have been implemented to tight-binding, combined to ab initio methods or fully implemented at a first principles level, enabling unprecedented quantitative exploration of charge transport in realistic models of materials and devices at the core of Nanosciences and Nanotechnology.

Dr. Roche has authored or co-authored more than 80 papers, bringing key contributions and reviews in journals with high impact. He has given more than forty keynotes and invited talks in International conferences such as Trends in Nanotechnology series (TNT), Nanotube NT series, APS march meeting, CARBON and ELECMOL conference series, and has been visiting researchers of IBM Watson Research Center (USA), Cambridge University (England), Donostia International Physics Center (Spain), Taiwanese Center for Theoretical Physics, and several Universities and organizations in Japan (Tokyo University, TITECH, NEC, AIST, Nihon University). His collaborations include the University of Dresden and Regensburg (Germany), the MIT and Rice University (USA), the Tokyo and Tohoku Universities (Japan). In 2009, he received the Alexander-von-Humboldt Friedrich Wilhelm Bessel Research Award in recognition of his contributions to the

field of Computational Nanosciences.

Fluent in many languages, Dr. Roche has dedicated genuine effort to strengthen international collaborations in the field of Nanosciences by organizing workshops and conferences, such as the Seventh edition of the series Trends in Nanotechnology (TNT2006), the Eight International Conference on Nanotubes (NT'08) and he is member of the organization committee of GRAPHENE 2011 (www.imaginenano.com). His strong belief in the benefits of an open exchange of scientific information is finally evidenced in his participation to the international GDR GNT research network on “Graphene and Nanotubes”, where he is in charge of promoting the networking activities in the fields of transport, field emission and devices. He is finally the coordinator of the French National project NANOSIM_GRAPHENE, funded by the ANR/PNANO programme (http://www.nanosimgraphene.org/) and dedicated on the development of new simulation tools to explore the properties of graphene-based devices.